REMARKS

The Examiner's action of January 12, 2009 finally rejecting the claims under 35USC103 as being unpatentable over the Bray patent is noted.

Applicant has amended the independent claims to recite that the interconnect layer is reprogrammable for defining a new function of the compute engine by redefining interconnects without reconfiguring the physical layer and thus without affecting the application layer and regardless of what is happening in the application layer.

If we take the physical layer to be the FPGA elements as mentioned in the specification, it is only with great difficulty that one can reconfigure FPGA elements to perform different functions. Note that according to the specification on page 2,

> "it usually takes 400 man-hours to generate an FPGA configuration, which is preceded by research and development typically on the order of 400 man-hours. Thus, for each mode of operation of the FPGAs, upwards of 800 man-hours are required.
>
> Where one wishing to change the mode of operation of the FPGAs in an electronics bay of an aircraft one would not want to completely reprogram each one of the FPGAs for each mode of operation, nor rewire the interconnects between the modules."

The way in the subject method that the reconfigurable compute engine has its function changed is not to touch the FPGAs, but rather to provide a programmable interconnect layer that redefines the interconnects without reconfiguring the physical layer, e.g. the FPGA apparatus.

First and foremost it can be seen that this type of control is nowhere shown or taught in the Bray reference. According to the Bray Abstract, "the methodology involves

monitoring signal detect inputs and based on their levels automatically reconfiguring the physical layer device. (emphasis supplied)

Since the Applicants claim that physical layer device is not reconfigured it would not be obvious how one would apply the Bray reference at all.

Moreover, the Bray system involves "monitoring signal detect inputs and based on their levels automatically reconfiguring..."

The signal detection input or SDI apparatus within Bray is in no way equivalent to programming or coding. Programming involves coding to achieve selected interconnect paths. This is the function of the claimed reconfigurable interconnect layer. In the claimed invention there is no monitoring of signal levels and any indication that the Bray system is equivalent to programming is spurious because recognition of signal levels is not equivalent in any way to coding or programming.

In short, the operation of the Bray device is to reconfigure physical layers. Applicants claim the opposite. Secondly, there is no such thing as a signal detect apparatus in the claimed invention; and certainly there is nothing in the Bray reference which has anything to do with programming or coding of the interconnect layer to interconnect different pins to different locations based on the programming.

For these reasons it is Applicant's contention that the independent claim is allowable and not obvious.

Thus, Applicants completely disagree with the Examiner that the SDI control circuit has anything to do with the claimed invention.

Moreover, the Examiner admits that "Bray fails to specifically teach that the interconnect layer is reprogrammable for defining a new function". Applicant agrees with the Examiner's analysis. Note, the Bray SDI control mechanism involves signal detection and reconfiguring the physical layer device, again which the claimed system avoids.

Additionally, the Examiner says that Bray fails to teach that the timing signals include a "strobe" and concludes that a strobe would be obvious. However, there is nothing to strobe in Bray. Therefore it is unclear how the Examiner can come to the conclusion that this is obvious.

The Examiner also says that Bray fails to teach that the different pins support the transmission of packet switched signals, the transmission of circuit switched signals, and discrete signal level transmissions. However without such a showing in Bray the claimed system cannot be obvious, both because what Bray fails to teach is admitted and because the Bray system does not operate in the same way the claimed system operates.

The Examiner says that Bray fails to teach that the predetermined functions include spatial processing, communication, signal intelligence and jamming. These elements are in no way equivalent to what Bray teaches as his modes of operation. The signal intelligence, spatial processing and communications functions are nowhere shown or taught in Bray and there is no reason to suggest why the PECL mode, 100 BASE-TX or 100 BASE-T modes, the loop back mode, or even the 100 BASE-FX modes are in any way equivalent to the claimed SIGINIT functions.

Moreover, the Examiner admits Bray fails to teach a FPGA. It is hard to see how one could equate anything in Bray with a field programmable gate array, because the system that Bray describes is one addressing the problems of local area networks, especially Ethernet networks. In Ethernet networks there are no countermeasure functions, no jamming functions, no signal intelligence functions, nor in fact anything that is flown around on an aircraft; and certainly does not involve field programmable gate arrays which are not used in Ethernet applications that connect traditional computers to each other.

It is Applicants' view that none of the claimed subject matter is obvious over Bray and that to the extent that claims 15-18 are method claims which loosely correspond to the apparatus claims, the method claims are likewise neither shown, taught nor obvious over Bray.

In view of the above Amendment, it is Applicants' contention that the claims are in condition for allowance. Allowance of the claims and issuance of the case is earnestly solicited. Alternatively, entry of this Amendment for purposes of appeal is requested.

Respectfully submitted,

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Date: March 11, 2009